Amendments to the Drawings:

The attached sheet of drawings includes changes to FIG. 2. In FIG. 2, previously omitted element 10 has been added.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS

This application has been carefully reviewed in light of the Office Action dated December 15, 2005. Claims 1-18 remain in this application. Claims 1-2 are the independent claims. Claims 1-2 have been amended. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Drawing Objections

The drawings were objected to under 37 C.F.R §1.83(a) for failing to show elements 10, 42 and 90 as described in the specification. In response, the drawings have been amended to comply with 37 C.F.R 1.83(a), and Applicant respectfully requests reconsideration of the drawings.

Specification Objections

The abstract was objected to under MPEP §608.01(b) for indefiniteness. In response, the abstract has been amended to comply with MPEP §608.01(b), and Applicant respectfully requests reconsideration of the abstract.

The disclosure was objected to for informalities. In response, the disclosure has been amended to correct informalities, and Applicant respectfully requests reconsideration of the disclosure.

The title was objected to for being non-descriptive. In response, the title has been amended accordingly, and Applicant respectfully requests reconsideration of the title.

Art-Based Rejections

Claims 1-2 and 13-14 were rejected under 35 U.S.C. §102(b) over US 5,655,096 (Branigin); Claims 3-12 and 15-18 were rejected under 35 U.S.C. §103(a) over Branigin in view of US 5,784,584 (Moore). Applicant respectfully traverses these rejections and submits that the claims herein are patentable in light of the clarifying amendments above and the arguments below.

The Branigin Reference

Branigin is directed to a computer processor that employs parallelism through pipelining by Sequential Coherency Instruction Scheduling and/or Sequential Coherency Exception Handling. *(See Branigin, Col. 15, lines 44-64).*

The Moore Reference

Moore is directed to a microprocessor that is directly connected to DRAMs and a microprocessor in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times. *(See Moore, Col. 1, line 59 to Col. 2, line 2).*

The Claims are Patentable Over the Cited References

The present application is generally directed to a data processing device using pipeline control.

As defined by amended independent Claim 1, a data processing device using pipeline control includes an instruction queue in which a plurality of instruction codes are fetched, a fetch address operation circuit which calculates a fetch address used to fetch an instruction code in the instruction queue, and a fetch circuit which fetches an instruction code that is read out based on the fetch address into the instruction queue. A branch information setting circuit decodes a branch setting

instruction which explicitly or implicitly implies information for specifying a branch address and a branch target address when the fetch address is a branch address after x-th instruction from the branch setting instruction. The branch information setting circuit stores the branch address in a branch address storage register and the branch target address in a branch target address storage register when the branch setting instruction is decoded. The fetch address operation circuit includes a circuit which compares one of a previous fetch address and an expected next fetch address with a value stored in the branch address storage register, and then determines whether or not to output a value stored in the branch target address storage register as a next fetch address, based on the comparison result.

The applied references do not disclose or suggest the above features of the present invention as defined by amended independent Claim 1. In particular, the applied references do not disclose or suggest, "a branch information setting circuit which decodes a branch setting instruction which explicitly or implicitly implies information for specifying a branch address and a branch target address when the fetch address is a branch address after x-th instruction from the branch setting instruction, the branch information setting circuit stores the branch address in a branch address storage register and the branch target address in a branch target address storage register, when the branch setting instruction is decoded", as required by amended independent Claim 1.

Branigin discloses a program counter that provides values for controlling the flow of a program by using a branch address when a branch instruction is successful or incrementing the previous history contents to form a new value. *(See Branigin, Col., 62, lines 54-59).* According to Branigin, a branch instruction is executed to access the source register and condition code, and the branch address or the value is selected by the program counter based on the success of the branch instruction. The

branch address resulting from the branch instruction is used to access another instruction from instruction memory. *(See Branigin, Col. 65, lines 17-32).*

In contrast to Branigin, the claims of the present invention require a branch information setting circuit that decodes a branch setting instruction which explicitly or implicitly implies information for specifying a branch address and a branch target address when the fetch address is a branch address after x-th instruction from the branch setting instruction. Moreover, the branch information setting circuit stores the branch address in a branch address storage register and the branch target address in a branch target address storage register when the branch setting instruction is decoded. A target instruction may be fetched in the instruction queue using a correct branch target address before the program counter value becomes a branch address. These features of the present invention are supported throughout the specification; for example, see Applicant's specification, page 7, lines 2-4 and page 15, lines 9-13.

Branigin does not disclose or suggest these features of the present invention as required by amended independent Claim 1. The ancillary Moore reference does not remedy the deficiencies of Branigin.

Since the applied references do not disclose or suggest the above features of the present invention as required by amended independent Claim 1, those references cannot be said to anticipate nor render obvious the invention which is the subject matter of that claim.

Accordingly, independent Claim 1, as amended, is believed to be in condition for allowance and such allowance is respectfully requested.

Amended independent Claim 2 is allowable for at least the same reasons as discussed above with reference to amended independent Claim 1 and such allowance is respectfully requested.

The remaining Claims 3-18 depend either directly or indirectly from amended independent Claims 1-2 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references. Thus, the remaining Claims 2-18 are also believed to be in condition for allowance and such allowance is respectfully requested.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: March 15, 2006

By: 

Dariush G. Adli
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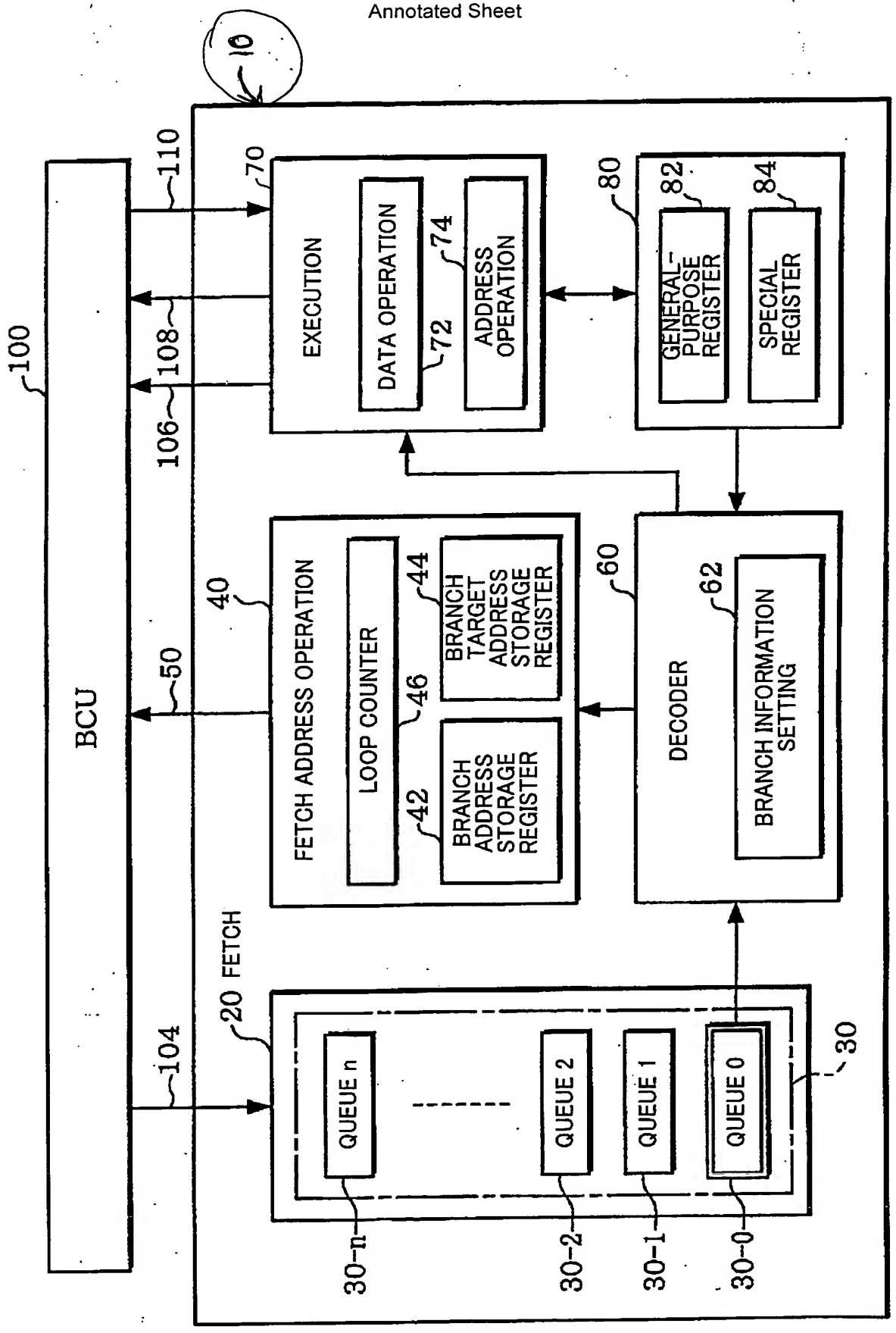

FIG. 2